

CLAIMS

The following is claimed:

- 1 1. A system for matching data and clock signal delays, comprising:
2 a clock buffer for driving said received clock signal to a register;
3 a data receiver for removing noise from received data; and
4 at least one miniature clock buffer, wherein said at least one miniature clock
5 buffer is a scaled version of said clock buffer, said miniature clock buffer having a
6 scaling factor of K, said scaling factor representing a number of said miniature clock
7 buffers utilized to minimize negative variations experienced by said clock buffer.
- 1 2. The system of claim 1, wherein said driving of said received clock
2 signal is performed by adding a gain factor to said received clock signal, thereby
3 increasing strength of said clock signal to allow propagation to said register.
- 1 3. The system of claim 1, wherein said clock buffer provides an amount
2 of delay that slows progression of said clock signal in a path to said register.
- 1 4. The system of claim 1, wherein said negative variations are selected
2 from the group consisting of process, voltage and temperature.
- 1 5. The system of claim 1, wherein said system is located within receive
2 logic situated on an application specific integrated circuit.

1 6. The system of claim 5, wherein a setup time of said receive logic is
2 represented by the equation:

$$3 \quad T_{\text{setup}} = T_{\text{reg-setup}} + 0.1 \times (-T_{\text{clk-dly}}) - T_{\text{clk-rte}(\text{min})}$$

4 wherein, $T_{\text{reg-setup}}$ is a setup time for said register, $T_{\text{clk-dly}}$ is a delay contributed by said
5 clock buffer, and $T_{\text{clk-rte}(\text{min})}$ is a minimum delay contributed by propagation of said
6 clock signal to said register.

1 7. The system of claim 5, wherein a hold time of said receive logic is
2 represented by the equation:

$$3 \quad T_{\text{hold}} = T_{\text{reg-hold}} + 0.1 \times (T_{\text{clk-dly}}) + T_{\text{clk-rte}(\text{max})}$$

4 wherein, $T_{\text{reg-hold}}$ is a hold time for said register, $T_{\text{clk-dly}}$ is a delay contributed by said
5 clock buffer, and $T_{\text{clk-rte}(\text{max})}$ is a maximum delay contributed by propagation of said
6 clock signal to said register.

1 8. A method of matching data and clock signal delays within receive
2 logic, comprising the steps of:

3 minimizing setup and hold times of said receive logic;

4 formulating at least one miniaturized version of a clock buffer located within
5 said receive logic, wherein said at least one miniaturized version of said clock buffer
6 is a scaled version of said clock buffer, said miniaturized version of said clock buffer
7 having a scaling factor of K, said scaling factor representing a number of said
8 miniaturized clock buffers utilized to minimize negative variations experienced by
9 said clock buffer; and

10 minimizing negative variations experienced by said clock buffer.

1 9. The method of claim 8, wherein said receive logic is situated on an
2 application specific integrated circuit.

1 10. The method of claim 8, wherein said negative variations are selected
2 from the group consisting of process, voltage and temperature.

1 11. The method of claim 8, wherein said clock buffer is capable of driving
2 a received clock signal to a register located within said receive logic.

1 12. The method of claim 11, wherein a setup time of said receive logic is
2 represented by the equation:

$$3 \quad T_{\text{setup}} = T_{\text{reg-setup}} + 0.1 \times (-T_{\text{clk-dly}}) - T_{\text{clk-rte}}(\text{min})$$

4 wherein, $T_{\text{reg-setup}}$ is a setup time for said register, $T_{\text{clk-dly}}$ is a delay contributed by said
5 clock buffer, and $T_{\text{clk-rte}}(\text{min})$ is a minimum delay contributed by propagation of said
6 clock signal to said register.

1 13. The method of claim 11, wherein a hold time of said receive logic is
2 represented by the equation:

$$3 \quad T_{\text{hold}} = T_{\text{reg-hold}} + 0.1 \times (T_{\text{clk-dly}}) + T_{\text{clk-rte}}(\text{max})$$

4 wherein, $T_{\text{reg-hold}}$ is a hold time for said register, $T_{\text{clk-dly}}$ is a delay contributed by said
5 clock buffer, and $T_{\text{clk-rte}}(\text{max})$ is a maximum delay contributed by propagation of said
6 clock signal to said register.

1 14. The method of claim 8, wherein said clock buffer provides an amount
2 of delay that slows progression of said clock signal in a path to a register located
3 within said receive logic.

1 15. A system for matching data and clock signal delays within receive
2 logic, comprising:
3 means for minimizing setup and hold times of said receive logic;
4 means for formulating at least one miniaturized version of a clock buffer
5 located within said receive logic, wherein said at least one miniaturized version of
6 said clock buffer is a scaled version of said clock buffer, said miniaturized version of
7 said clock buffer having a scaling factor of K, said scaling factor representing a
8 number of said miniaturized clock buffers utilized to minimize negative variations
9 experienced by said clock buffer; and
10 means for minimizing negative variations experienced by said clock buffer.

1 16. The system of claim 15, wherein said receive logic is situated on an
2 application specific integrated circuit.

1 17. The system of claim 15, wherein said negative variations are selected
2 from the group consisting of process, voltage and temperature.

1 18. The system of claim 15, wherein said clock buffer is capable of driving
2 a received clock signal to a register located within said receive logic.

1 19. The system of claim 18, wherein a setup time of said receive logic is
2 represented by the equation:

3
$$T_{\text{setup}} = T_{\text{reg-setup}} + 0.1 \times (-T_{\text{clk-dly}}) - T_{\text{clk-rte}}(\text{min})$$

4 wherein, $T_{\text{reg-setup}}$ is a setup time for said register, $T_{\text{clk-dly}}$ is a delay contributed by said
5 clock buffer, and $T_{\text{clk-rte}}(\text{min})$ is a minimum delay contributed by propagation of said
6 clock signal to said register.

1 20. The system of claim 18, wherein a hold time of said receive logic is
2 represented by the equation:

3
$$T_{\text{hold}} = T_{\text{reg-hold}} + 0.1 \times (T_{\text{clk-dly}}) + T_{\text{clk-rte}}(\text{max})$$

4 wherein, $T_{\text{reg-hold}}$ is a hold time for said register, $T_{\text{clk-dly}}$ is a delay contributed by said
5 clock buffer, and $T_{\text{clk-rte}}(\text{max})$ is a maximum delay contributed by propagation of said
6 clock signal to said register.